Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	287963	(ARC or (anti adj reflective) or (anti adj reflection) or (anit adj reflecting))	US-PGPUB; USPAT	OR	ON	2005/10/27 10:04
L2	3289	1 and memory and logic and (mask or photoresist or resist)	US-PGPUB; USPAT	OR	ON	2005/10/27 08:22
L3	2500	2 and (etching or removing or etch or remove)	US-PGPUB; USPAT	OR	ON	2005/10/27 08:22
L4	217	3 and (thickness with (ARC or (anti adj reflective) or (anti adj reflection) or (anit adj reflecting)))	US-PGPUB; USPAT	OR	ON	2005/10/27 08:27
L5	29	4 and ((silicon adj oxynitride) with (ARC or (anti adj reflective) or (anti adj reflection) or (anit adj reflecting)))	US-PGPUB; USPAT	OR	ON	2005/10/27 08:24
L6	188	4 not 5	US-PGPUB; USPAT	OR	ON	2005/10/27 09:30
L9	4449	438/636,637,700,725,749.ccls.	US-PGPUB; USPAT	OR	ON	2005/10/27 10:02
L10	934	9 and (ARC or (anti adj reflective) or (anti adj reflection) or (anit adj reflecting))	US-PGPUB; USPAT	OR	ON	2005/10/27 10:03
L11	918	10 not 4	US-PGPUB; USPAT	OR	ON	2005/10/27 10:03
L12	607	11 and @ad<"20020219"	US-PGPUB; USPAT	OR	ON	2005/10/27 10:04
L13	23	((ARC or (anti adj reflective) or (anti adj reflection) or (anit adj reflecting)) and memory and logic and (resist or photoresist or mask)).clm.	US-PGPUB; USPAT	OR	ON	2005/10/27 10:13
L14	8	13 and @ad<"20020219"	US-PGPUB; USPAT	OR	ON	2005/10/27 10:05
L16	91	((ARC or (anti adj reflective) or (anti adj reflection) or (anit adj reflecting)) and memory and logic and (resist or photoresist or mask))	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/27 10:13

DOCUMENT-IDENTIFIER: US 20010010976 A1

TITLE: Method and system for reducing ARC layer removal bamd providing a capping layer for the ARC layer

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Claims Text - CLTX (2):
1. A method providing a semiconductor device comprising the steps of: (a) providing an antireflective coating (**ARC**) layer having antireflective properties, at least a portion of the **ARC** layer being on the first layer; and (b) providing a capping layer on the **ARC** layer, the capping layer reducing a susceptibility of the **ARC** layer to removal while allowing the **ARC** layer to substantially retain the antireflective properties.

Claims Text - CLTX (3):
2. The method of claim 1 wherein the **ARC** layer providing step (a) further includes the steps of: (a1) depositing the **ARC** layer.

Claims Text - CLTX (5):
4. The method of claim 1 wherein the capping layer providing step (b) further includes the step of: (b1) providing a capping layer having a capping layer thickness that is sufficient to reduce the susceptibility of the **ARC** layer to removal without substantially affecting the antireflective properties of the **ARC** layer.

Claims Text - CLTX (8):
7. The method of claim 6 wherein the **ARC** layer is a SiON **ARC** layer and wherein a thickness of the SiON **ARC** layer is three hundred Angstroms plus or minus no more than approximately ten percent.

Claims Text - CLTX (9):
8. The method of claim 4 wherein the susceptibility of removal of the **ARC** layer is a susceptibility to removal in a wet **photoresist** strip.

Claims Text - CLTX (10):
9. A semiconductor device comprising: a plurality of **memory** cells; wherein the plurality of **memory** cells are defined using an antireflective coating (**ARC**) layer and a capping layer covering the **ARC** layer, the **ARC** layer having antireflective properties, the capping layer reducing a susceptibility of the

ARC layer to removal while allowing the ARC layer to substantially retain the antireflective properties.

Claims Text - CLTX (11):
10. The semiconductor device of claim 9 wherein the capping layer further has a capping layer thickness that is sufficient to reduce the susceptibility of the ARC layer to removal without substantially affecting the antireflective properties of the ARC layer.

Claims Text - CLTX (14):
13. The semiconductor device of claim 12 wherein the ARC layer is a SiON ARC layer and wherein a thickness of the SiON ARC layer is three hundred Angstroms plus or minus no more than approximately ten percent.

Claims Text - CLTX (15):
14. The semiconductor device of claim 10 wherein the susceptibility of removal of the ARC layer is a susceptibility to removal in a wet **photoresist** strip.

Claims Text - CLTX (16):
15. The semiconductor device of claim 7 further comprising: a plurality of **logic** cells; wherein the plurality of **logic** cells are defined using the ARC layer and a capping layer covering the ARC layer, the ARC layer having antireflective properties, the capping layer reducing a susceptibility of the ARC layer to removal while allowing the ARC layer to substantially retain the antireflective properties.